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1 1. (Twice Amended) An integrated circuit device comprising:  
2 a conductive pad to receive an input signal from an external signal line;  
3 a first doped region of a first conductivity type disposed in a semiconductor substrate of a  
4 second conductivity type, wherein the first doped region is underlying and surrounding the  
5 conductive pad;  
6 a conductive region of the first conductivity type disposed in the first doped region;  
7 a first tap region spaced apart from and surrounding a substantial portion of the first  
8 doped region, wherein the first tap region is electrically coupled to a first supply voltage;  
9 an output driver transistor having a drain region and a source region, wherein the drain  
10 region is electrically coupled to the conductive pad; and  
11 a second tap region surrounding the output driver transistor, wherein the second tap  
12 region is electrically and physically coupled to a second supply voltage and the source region.

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1 2. The integrated circuit device of claim 1 wherein the first and second supply voltages  
2 are ground.

1 3. The integrated circuit device of claim 2 wherein the first tap region completely  
2 surrounds the first doped region.

1 4. The integrated circuit device of claim 1 wherein the first tap region is a discontinuous  
2 region.

1 5. (Twice Amended) The integrated circuit device of claim 1 wherein a doping  
2 concentration of the first doped region is less than a doping concentration of the conductive  
3 region.

1 6. (Amended) The integrated circuit device of claim 1 wherein the first tap region is a  
2 second doped region and the second tap region is a third doped region.

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1 7. (Twice Amended) The integrated circuit device of claim 6 wherein the second doped  
2 region is of an opposite conductivity type than the first doped region.

1 8. (Twice Amended) The integrated circuit device of claim 6 wherein the third doped  
2 region is a P type doped region and the output driver transistor is an NMOS type transistor.

1 9. (Amended) The integrated circuit device of claim 1 further including a tap region  
2 portion that is spaced apart from and surrounding the first doped region, wherein the tap region  
3 portion is decoupled from the first supply voltage to provide a predetermined resistance between  
4 the first doped region and the first supply voltage.

1 10. (Twice Amended) The integrated circuit device of claim 1 wherein a portion of the  
2 second tap region is integrated into the source region.

1 11. The integrated circuit device of claim 10 wherein the first tap region is a  
2 discontinuous region.

1 12. (Twice Amended) A bond pad for an integrated circuit device, the bond pad  
2 comprising:

3 a conductive bonding layer;

4 a doped region of a first conductivity type formed in a semiconductor substrate of a  
5 second conductivity type, wherein the doped region is underlying and surrounding the  
6 conductive bonding layer;

C 7 a conductive region of the first conductivity type disposed in the doped region, wherein  
8 the conductive region is underlying the conductive bonding layer and wherein the conductive  
9 region includes a surface area at least substantially equal to a surface area of the conductive  
10 bonding layer; and

11 a conductive tap region spaced apart from and surrounding at least a portion of the doped  
12 region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

1 13. The bond pad of claim 12 wherein the supply voltage is a ground voltage and the  
2 conductive bonding layer includes a metal.

1 14. (Twice Amended) The bond pad of claim 12 wherein the doping concentration of the  
2 doped region is less than the doping concentration of the conductive region.

1 15. (Amended) The bond pad of claim 12 wherein the conductive tap region is doped to  
2 be of an opposite conductivity type than the first doped region.

1        16. (Amended) The bond pad of claim 12 further including a conductive tap region  
2        portion that is spaced apart from and surrounding the doped region, wherein the conductive tap  
3        region portion is decoupled from the supply voltage to provide a predetermined resistance  
4        between the doped region and the supply voltage.

1        17. The bond pad of claim 12 wherein the conductive tap region is a continuous region.

C' 1        18. (Twice Amended) The bond pad of claim 17 wherein the conductive tap region  
2        completely surrounds the doped region.

1        19. The bond pad of claim 12 wherein the conductive tap region is a discontinuous  
2        region.

1        20. The bond pad of claim 19 wherein the conductive tap region substantially surrounds  
2        the doped region in a concentric-like manner.

1        21. The bond pad of claim 12 wherein the conductive region is polysilicon.

1        22. (Amended) The bond pad of claim 21 wherein the conductive tap region is a doped  
2        layer positioned beneath the conductive region.

1 23. (Twice Amended) A transistor layout for an integrated circuit device having a bond  
2 pad, the transistor layout comprising:

3 a drain region having a first conductivity type doping, wherein the drain region is formed  
D2 4 in a semiconductor substrate region having a second conductivity type doping, the drain region  
5 being electrically coupled to the bond pad;

6 a source region including a second conductivity type doping; and

7 a conductive tap region spaced proximal to and surrounding the drain region, wherein the  
8 conductive tap region is electrically coupled to a supply voltage and electrically and physically  
C1 9 coupled to the source region.

1 24. (Amended) The transistor layout of claim 23 wherein the supply voltage is a ground  
2 voltage.

1 26. The transistor layout of claim 23 wherein the conductive tap region is spaced  
2 proximal to and completely surrounds the drain region.

1 27. The transistor layout of claim 23 wherein the conductive tap region is a  
C1 2 discontinuous region.

1 28. The transistor layout of claim 23 further including:

2 a plurality of source regions, each source region of the plurality of source regions being  
3 electrically and physically coupled to the conductive tap region;

4 a plurality of drain regions, each drain region of the plurality of drain regions being  
5 electrically coupled to the bond pad; and

6 wherein the conductive tap region is spaced proximal to and surrounds at least one drain

C1 7 region of the plurality of drain regions.

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Kindly ADD the following claims:

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1 29. (New) The transistor layout of claim 23 wherein the source region includes the first  
2 conductivity type doping.

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2 contiguous through a length of the source region.

1 31. (New) The transistor layout of claim 23 further including a conductive tap region  
2 portion spaced proximal to the drain region, wherein the conductive tap region portion is  
3 electrically decoupled from the supply voltage and physically decoupled from the conductive tap  
4 region.

1 32. (New) The transistor layout of claim 31 wherein the conductive tap region portion is  
2 electrically decoupled from the supply voltage and physically decoupled from the conductive tap  
3 region using a metal mask option.

1 33. (New) The transistor layout of claim 23 wherein the first conductivity type doping is  
2 N type doping and the second conductivity type doping is P type doping.

1 34. (New) The integrated circuit device of claim 9 wherein the tap region portion is  
2 physically separate from the first tap region.

1 35. (New) The integrated circuit device of claim 16 wherein the conductive tap region  
2 portion is decoupled from the first supply voltage using a metal mask option.

C2 1 36. (New) The bond pad of claim 16 wherein the conductive tap region portion is  
2 physically separate from the conductive tap region.

1 37. (New) The bond pad of claim 16 wherein the conductive tap region portion is  
2 decoupled from the supply voltage using a metal mask option.

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